Reg No.:_____ Name:____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth semester B.Tech examinations (S), September 2020

Course Code: EC212

Course Name: LINEAR INTEGRATED CIRCUITS AND DIGITAL ELECTRONICS (MC)

Max. Marks: 100 Duration: 3 Hours

PART A

		PART A		
	- 0	Answer all the questions below; each one carries 5 marks.	Marks	
1	Defi	ine the following terms and explain their significance in practical circuits	(5)	
		(i) Input offset Voltage		
	((ii) CMRR		
2	Hov	Iow can we use op amp as peak detector (5)		
3	Disc	Discuss briefly about narrow band pass filter. (5		
4	Con	vert the following	(5)	
	a) [4	$[468]_{10} = []_2$		
	b) [$[10101011]_2 = []_{16}$		
	c) [2	$[237]_8 = []_{10}$		
	d) [A	$A3B6]_{16} = [$ $]_2$		
5	Des	ign and implement a half adder with minimum number of gates.	(5)	
6	Compare the characteristics of RAM and ROM.			
7	Distinguish between combinational and sequential circuits.			
8	Discuss briefly about race around condition in JK flip flop.			
		PART B		
		Answer any three full questions; each carries 10 marks.		
9		Demonstrate any two applications of op amp.	(10)	
10	(a)	Illustrate any two applications of op amp as comparator.	(5)	
	(b)	Draw the circuit diagram and show that op amp can be used as log amplifier.	(5)	
11	(a)	Illustrate the working principle of an weighted resistor type D/A converter.	(6)	
	(b)	With neat circuitry explain the working of flash type ADC.	(4)	
12		Simplify the following SOP function using Karnaugh map and implement with	(10)	
		basic logic gates		
		$F(A,B,C,D) = \Sigma m(2,3,6,7,8,10,11,12) + d(14,15)$		

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13	Elucidate the working of a monostable multivibrator with a circuit diagram and	(10)
	waveform.	
	PART C Answer any two full questions; each carries 15 marks.	
14	Design the following combinational circuits	(15)
	i) 8X1 MUX	
	ii) 1X8 DEMUX	
15	Design and implement a 3-bit gray to binary code converter.	(15)
16	Obtain the characteristic equation and explain the following	(15)
	i) D- flipflop	
	ii) T - flipflop	
17	Summarize the following	(15)
	i) SISO	
	ii) SIPO	
